

Fig. 1

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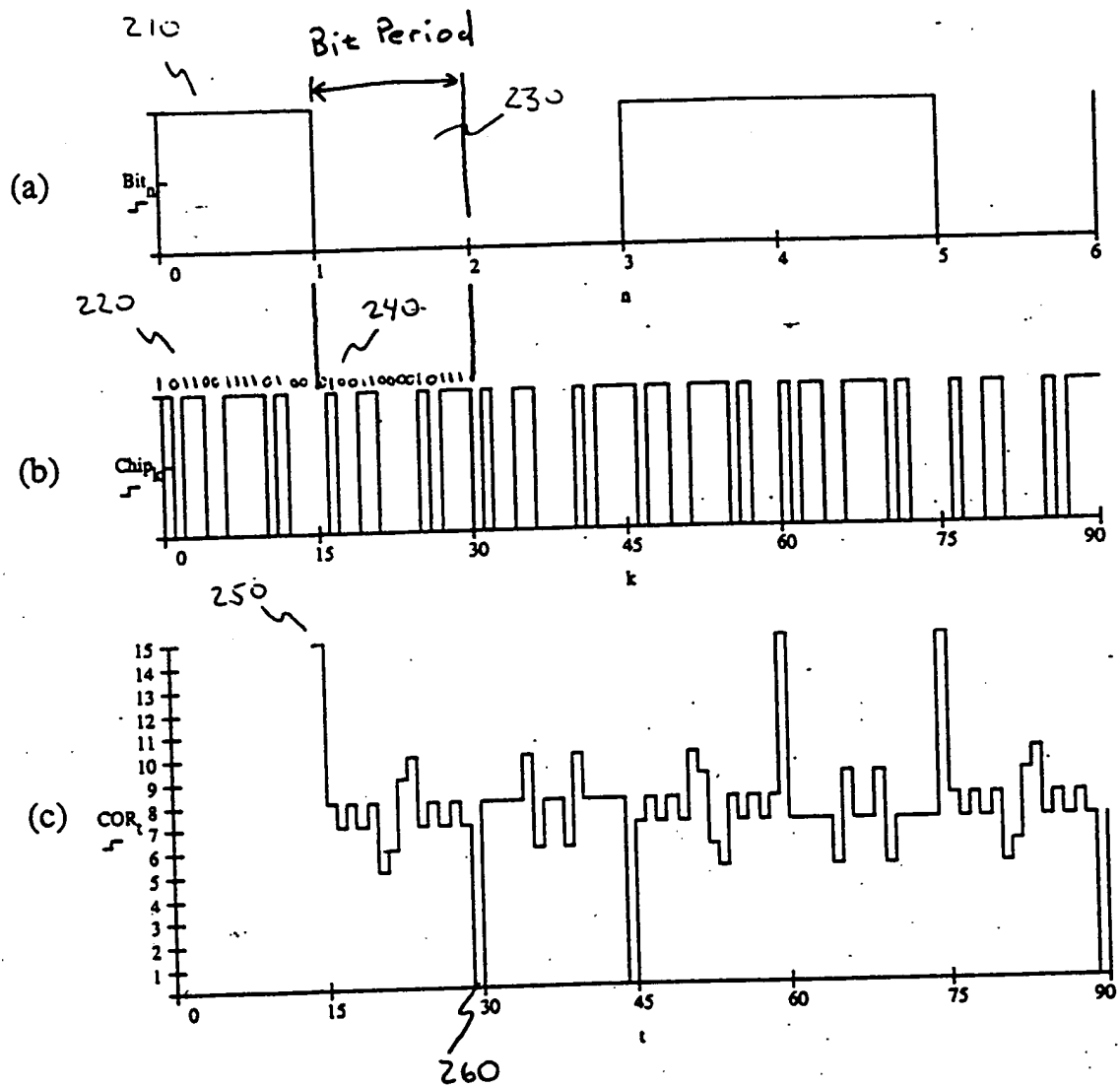


Fig. 2.

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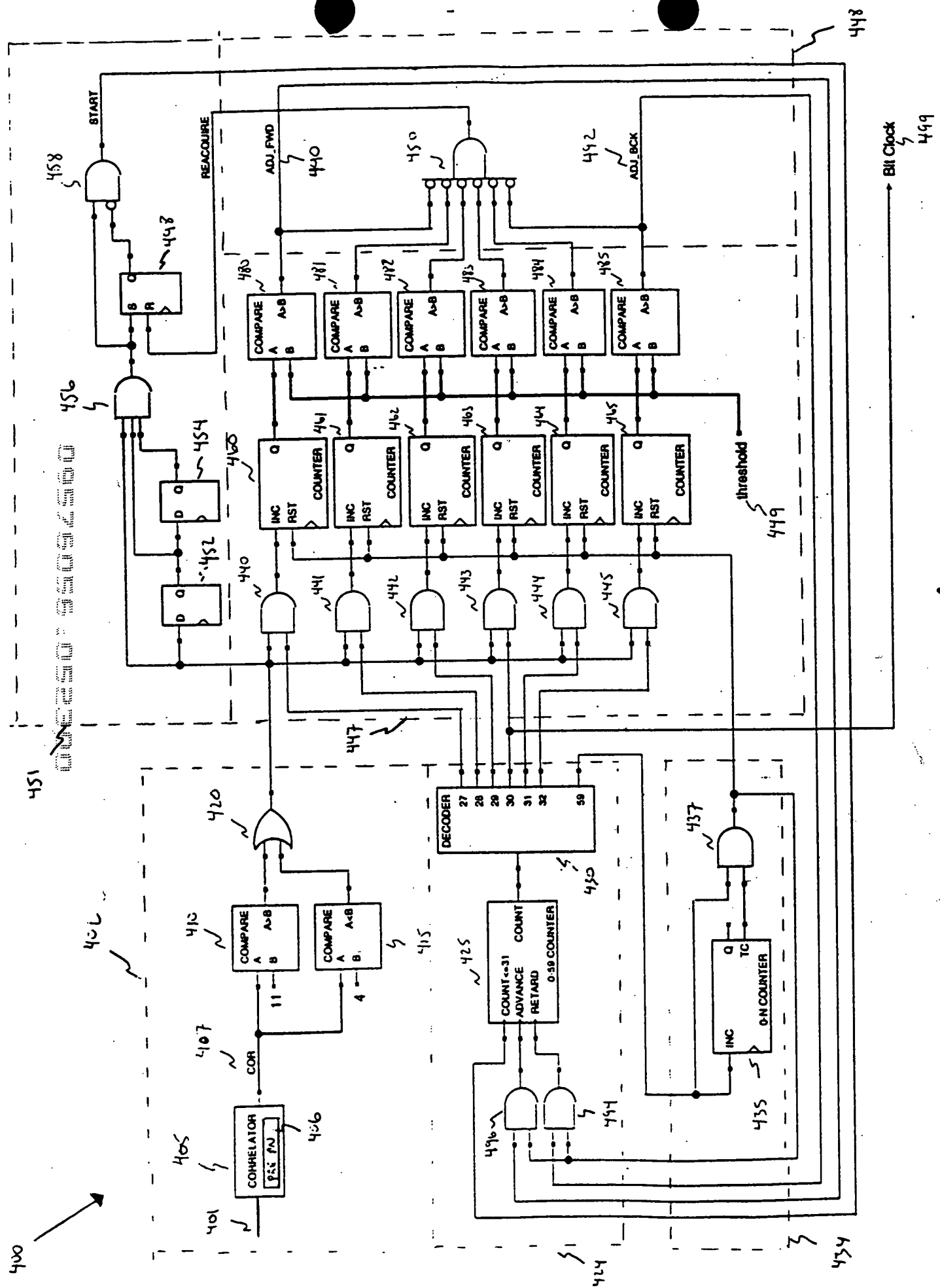
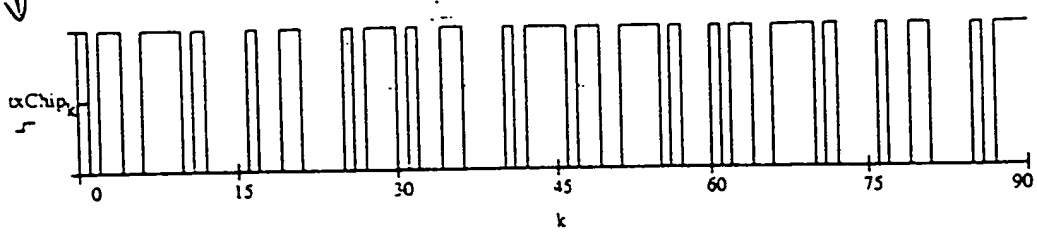


Fig. 4

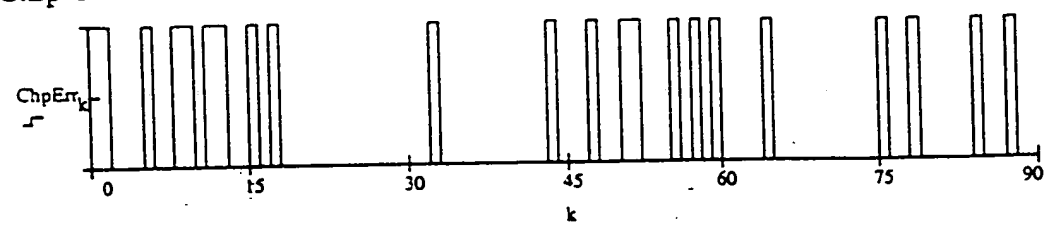
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↓

(a)

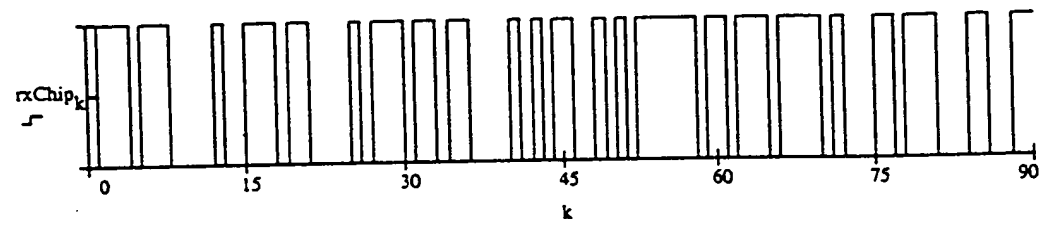


Chip Error Rate = 0.2

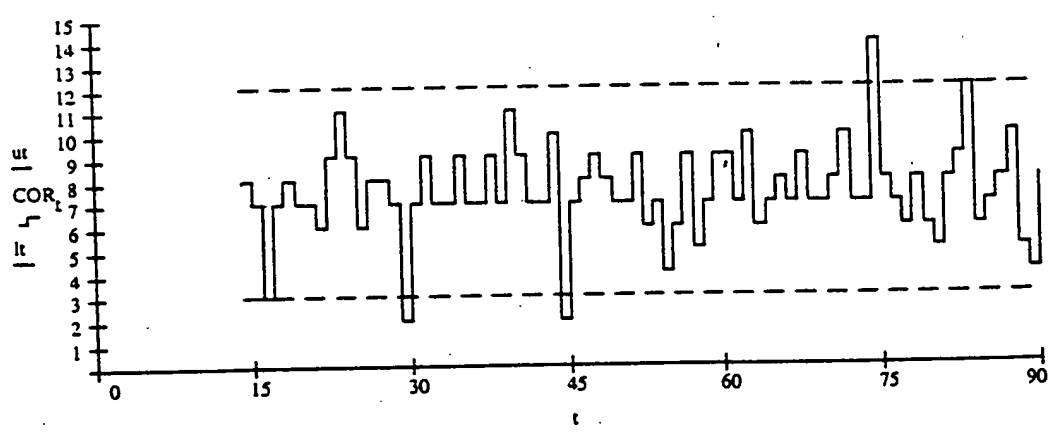
(b)



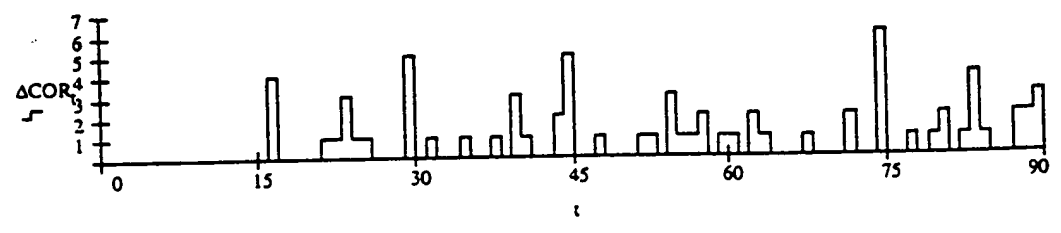
(c)



(d)



(e)



(f)

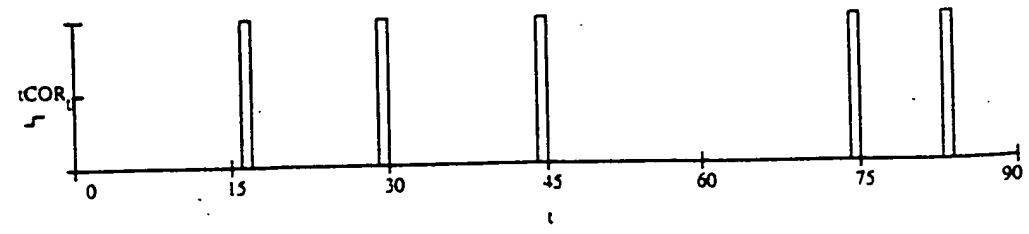


Fig. 5

